IN THE SPECIFICATION

Please amend the specification as follows:

Replace the paragraph on page 8, between lines 3-9 of the specification with the following:

Figure 4 is a block diagram schematically showing relevant components of a disc drive according to a preferred embodiment of the invention. In this embodiment, the control circuit 90 comprises four controllable filter devices ~~110a, 110b, 110c, 110d~~ 110A, 110B, 110C, 110D, having respective outputs ~~112a, 112b, 112c, 112d~~ 112A, 112B, 112C, 112D, and having respective inputs ~~111a, 111b, 111c, 111d~~ 111A, 111B, 111C, 111D coupled to the respective signal inputs ~~91a, 91b, 91c, 91d~~ 91A, 91B, 91C, 91D of the control circuit 90. Further, the control circuit 90 comprises two delay calculators 120 and 130, having respective outputs 123 and 133.

Replace the paragraph on page 8, between lines 10-14 of the specification with the following:

The first delay calculator 120 has a first input 121 coupled

to the output ~~112a~~ 112A of the first controllable filter device ~~110a~~ 110A, and has a second input 122 coupled to the output 112d of the fourth controllable filter device ~~110d~~ 110D. At its output 123, the first delay calculator 120 provides a signal S1 representing the delay $\Delta(A,D)$ between the signals A and D of the first and fourth detector segments 35a and 35d, respectively.

Replace the paragraph on page 8, between lines 15-19 of the specification with the following:

The second delay calculator 130 has a first input 131 coupled to the output ~~112b~~ 112C of the ~~second~~ third controllable filter device ~~110b~~ 110B, and has a second input ~~122~~ 132 coupled to the output ~~112c~~ 112B of the ~~third~~ fourth controllable filter device ~~110c~~ 110B. At its output 133, the second delay calculator 130 provides a signal S2 representing the delay $\Delta(B,C)$ between the signals B and C of the second and third detector segments 35b and 35c, respectively.

Replace the paragraph on page 8, between lines 25-32 of the

specification with the following:

Further, the control circuit 90 comprises a second adder 150, having four inputs ~~151a, 151b, 151c, 151d~~ 151A, 151B, 151C, 151D coupled to the respective signal inputs ~~91a, 91b, 91c, 91d~~ 91A, 91B, 91C, 91D of the control circuit 90. At an output 152, the second adder 150 provides a signal S4 representing the central aperture signal CA of the optical detector 35, i.e. the sum signal of the four detector quadrants. Further, the control circuit 90 comprises a filter controller 160, having an input 161 coupled to receive the output signal S4 of the second adder 150. The filter controller 160 has an output 162, coupled to respective control inputs ~~113a, 113b, 113c, 113d~~ 113A, 113B, 113C, 113D of the controllable filters ~~110a, 110b, 110c, 110d~~ 110A 110B, 110C, 110D.

Replace the paragraph on page 9, between lines 1-3 of the specification with the following:

Alternatively, the filter controller 160 may have four separate outputs ~~162a, 162b, 162c, 162d (not shown)~~, each coupled to the respective control inputs of the controllable filters ~~110a, 110b, 110c, 110d~~ 110A, 110B, 110C, 110D.

Replace the paragraph on page 12, between lines 13-21 of the specification with the following:

Figure 7 is a block diagram schematically illustrating an alternative embodiment of the control circuit, indicated at reference numeral 290. In this embodiment, the control circuit 290 comprises a first branch of filter devices ~~310a to 310d~~ 310A, 310B, 310C, 310D, delay detectors 320, 330, and adder 340, connected in a manner comparable to the circuit described above with reference to control circuit 90 (figure 4). These components may be identical to the components 110, 120, 130, 140 in the above-described embodiment of control circuit 90, with the exception that the filter devices ~~310a to 310d~~ 310A, 310B, 310C, 310D do not need to be controlled and therefore do not need to be controllable filter devices; in fact, these filter devices 310a to 310d may each be identical to the first filter 115 described above.

Replace the paragraph on page 12, between lines 22-28 of the specification with the following:

Further, in this embodiment, the control circuit 290 comprises

a second branch of filter devices ~~410a to 410d~~ 410A, 410B, 410C, 410D, delay detectors 420, 430, and adder 440, connected in a manner comparable to the first branch. Likewise, these components may be identical to the components 110, 120, 130, 140 in the above-described embodiment of control circuit 90, with the exception that the filter devices 410a to 410d are not controlled and therefore do not need to be controllable filter device; in fact, these filter devices ~~410a to 410d~~ 410A, 410B, 410C, 410D may each be identical to the second filter 116 described above.

Replace the paragraph on page 12, between lines 29-33 of the specification with the following:

The filter devices ~~310a to 310d~~ 310A, 310B, 310C, 310D and the filter devices ~~410a to 410d~~ 410A, 410B, 410C, 410D have their respective inputs ~~311a-d and 411a-d~~ connected in parallel to the respective inputs ~~291a-d~~ 291A, 291B, 291C, 291D of the control circuit 290. Thus, the first adder 340 of the first branch provides the wobble-derived DTD4 signal, while the second adder 440 of the second branch provides the data-derived DTD4 signal.

Replace the paragraph on page 13, between lines 19-28 of the specification with the following:

Figure 8 is a block diagram which schematically shows how this functionality can be implemented in a delay calculator, for example delay calculator 120. The delay calculator device 120 of this example comprises a controllable switch 125, having a first input 125a coupled to the second device input 122, a second input ~~125b~~ 125B, a control input ~~125c~~ 125C coupled to the device control input 124, and an output ~~125d~~ 125D. The delay calculator device 120 of this example further comprises an inverter 127, having its input coupled to the second device input 122 and having its output coupled to the second input ~~125b~~ 125B of the controllable switch 125. The controllable switch 125 is designed to connect its output ~~125d~~ 125D to either its first input ~~125a~~ 125A or its second input ~~125b~~ 125B, depending on the value of the signal received at its control input ~~125c~~ 125C.

Replace the paragraph on page 13, between lines 29-34 of the specification with the following:

The delay calculator device 120 of this example further

comprises an actual delay calculating unit 126, having a first input ~~126a~~ 126A coupled to the first device input 121, a second input ~~126b~~ 126B coupled to the output 125d of the controllable switch 125, and an output ~~126c~~ 126C coupled to the device output 123, which actual delay calculating unit 126 is designed to calculate the delay between the signals arriving at its two inputs and generating an output signal representing this delay.